IN THE CLAIMS:

[c1] (Currently amended) An integrated circuit device having a memory area comprising a data memory, ~~characterized in that~~ wherein said data memory has at least one counter element, at least one indicator element and at least one threshold value, wherein said counter element, on the one hand, counts at least one occurrence number of events occurring within said device and, on the other hand, can reach said threshold value, which is indicative of a large maximum number of occurrences of said events, said indicator element being designed to go from a first state to a second state when said counter element has reached said threshold value.

[c2] (Currently amended) ~~A~~The device according to claim 1, ~~characterized in that~~ wherein an event is an action occurring within said device which leads to a result and whose mean number of occurrences during the lifetime of said device can be determined.

[c3] (Currently amended) ~~A~~The device according to ~~any one of the preceding claims~~ claim 1, ~~characterized in that~~ wherein said threshold value represents an unlikely number of occurrences of said events occurring within said device during normal use of said device.

[c4] (Currently amended) ~~A~~The device according to ~~any one of the preceding claims~~ claim 1, ~~characterized in that~~ wherein a threshold value is defined for each counter element.

[c5] (Currently amended) ~~A~~The device according to ~~any one of the preceding claims~~ claim 1, ~~characterized in that~~ wherein a counter element is defined for a unique event.

[c6] (Currently Amended) ~~A~~The device according to ~~any one of claims 1 to 4~~ claim 1, ~~characterized in that~~ wherein a counter element is defined for at least two events.

[c7] (Currently Amended) ~~A~~The device according to ~~any one of the preceding claims~~ claim 1, ~~characterized in that~~ wherein at least one indicator element is defined for a unique counter element.

[c8] (Currently Amended) ~~A~~The device according to ~~any one of claims 1 to 6~~ claim 1, ~~characterized in that~~ wherein at least one indicator element is defined for at least two counter elements.

[c9] (Currently Amended) ~~A~~The device according to ~~any one of the preceding claims~~ claim 1, ~~characterized in that~~ wherein said data memory contains at least two indicator elements at non-contiguous locations within said data memory.

[c10] (Currently Amended) ~~A~~The device according to ~~any one of the preceding claims~~ claim 1, ~~characterized in that~~ wherein said memory area comprises means for disabling the operation of said device when an indicator element has gone to the second state.

[c11] (Currently Amended) ~~A~~The device according to claims ~~9 and~~ 10, ~~characterized in that~~ wherein disabling means disable the operation of said device when the state of one indicator element is different from the state of another identical indicator element.

[c12] (Currently Amended) ~~A~~The device according to ~~any one of the preceding claims~~ claim 1, ~~characterized in that~~ wherein said large maximum number of event occurrences is greater than about one hundred, and preferably, greater than about one thousand.